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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,433	05/24/2006	Yongxun Liu	290836US2PCT	2549

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EXAMINER
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ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
12/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/580,433	LIU ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The Information Disclosure Statement(s) filed on 24 May 2006 has been considered.

Oath/Declaration

The oath or declaration filed on 24 May 2006 is acceptable.

Drawings

Figures 27(A)-29 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhu et al. (US 2005/0110085 A1).

With respect to claim 1, Zhu et al. (Fig. 2L) discloses a dual-gate field effect transistor comprising a substrate [122], a source [paragraph 0024], a drain [paragraph 0024], a vertical channel provided between the source and the drain as rising from the substrate [paragraph 0024], a pair of gate insulation films [140, 146] sandwiching the channel from a direction orthogonal to a carrier-running direction in the channel and a pair of gate electrodes [160, 162] facing the channel, respectively, via the pair of gate insulation films, wherein the pair of insulation films have different thicknesses [paragraph 0023].

With respect to claim 2, Zhu et al. discloses a dual-gate field effect transistor according to claim 1. Zhu et al. further discloses the pair of gate electrodes are electrically connected to each other [paragraph 0031].

With respect to claim 3, Zhu et al. discloses a dual-gate field effect transistor according to claim 1. Zhu et al. further discloses the pair of gate electrodes are electrically independent of each other [paragraph 0031].

With respect to claim 4, Zhu et al. discloses a dual-gate field effect transistor according to claim 1. Zhu et al. further discloses the pair of gate insulation films have different permittivities [paragraph 0023].

With respect to claim 7, Zhu et al. (FIg. 2L) discloses a dual-gate field effect transistor comprising a substrate [122], a source [paragraph 0024], a drain [paragraph 0024], a vertical channel provided between the source and the drain as rising from the substrate [paragraph 0024], a pair of gate insulation films [140, 146] sandwiching the channel from a direction orthogonal to a carrier-running direction in the channel and a pair of gate electrodes [160, 162] facing the channel, respectively, via the pair of gate insulation films, wherein the pair of insulation films have different permittivities [paragraph 0023].

With respect to claim 8, Zhu et al. discloses a dual-gate field effect transistor according to claim 7. Zhu et al. further discloses the pair of gate electrodes are electrically connected to each other [paragraph 0031].

With respect to claim 9, Zhu et al. discloses a dual-gate field effect transistor according to claim 7. Zhu et al. further discloses wherein the pair of gate electrodes are electrically independent of each other [paragraph 0031].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. in view of Mathew et al. (US 6,903,967 B2).

With respect to claim 5, Zhu et al. discloses the dual-gate field effect transistor according to claim 1. Zhu et al. does not specify the pair of gate electrodes have different work functions.

However, Mathew et al. (Figs. 15, 16) discloses it is well known in the art for a pair of gate electrodes [1503, 1505] to have different work functions [column 8 lines 54-58]. Mathew et al. teaches it is beneficial for a pair of gate electrodes to have different work functions in order to control the voltage threshold of the device [column 8 lines 46-58].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the pair of gate electrodes of Zhu et al. to have different work functions, such as taught by Mathew et al., in order to control the voltage threshold of the device.

With respect to claim 10, Zhu et al. discloses a dual-gate field effect transistor according to claim 7. Zhu et al. does not specify the pair of gate electrodes have different work functions.

However, Mathew et al. (Figs. 15, 16) discloses it is well known in the art for a pair of gate electrodes [1503, 1505] to have different work functions [column 8 lines 54-58]. Mathew et al. teaches it is beneficial for a pair of gate electrodes to have different work functions in order to control the voltage threshold of the device [column 8 lines 46-58].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the pair of gate electrodes of Zhu et al. to have different work functions, such as taught by Mathew et al., in order to control the voltage threshold of the device.

With respect to claim 12, Zhu et al. discloses a dual-gate field effect transistor comprising a a substrate [122], a source [paragraph 0024], a drain [paragraph 0024], a vertical channel provided between the source and the drain as rising from the substrate [paragraph 0024], a pair of gate insulation films [140, 146] sandwiching the channel from a direction orthogonal to a carrier-running direction in the channel and a pair of gate electrodes [160, 162] facing the channel, respectively, via the pair of gate insulation films [paragraph 0023]. Zhu et al. does not specify the pair of gate electrodes have different work functions.

However, Mathew et al. (Figs. 15, 16) discloses it is well known in the art for a pair of gate electrodes [1503, 1505] to have different work functions [column 8 lines 54-58]. Mathew et al. teaches it is beneficial for a pair of gate electrodes to have different work functions in order to control the voltage threshold of the device [column 8 lines 46-58].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the pair of gate electrodes of Zhu et al. to have different work functions, such as taught by Mathew et al., in order to control the voltage threshold of the device.

With respect to claim 13, Zhu et al. in view of Mathew et al. discloses a dual-gate field effect transistor according to claim 12. Zhu et al. further discloses the pair of gate electrodes are electrically connected to each other [paragraph 0031].

With respect to claim 14, Zhu et al. in view of Mathew et al. discloses a dual-gate field effect transistor according to claim 12. Zhu et al. further discloses wherein the pair of gate electrodes are electrically independent of each other [paragraph 0031].

Claims 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. in view of Matsuoka (JP 02-015675 A).

With respect to claim 6, Zhu et al. discloses a dual-gate field effect transistor according to claim 1. Zhu et al. does not specify that the vertical channel has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively.

However, Matsuoka (Figs. 1(a), 1(b) discloses a vertical channel [15] has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films [17] are in contact with slant faces that are opposed sides of the triangle, respectively [Abstract]. Matsuoka teaches it is beneficial for a vertical channel to have a triangle shape in cross section in the direction

orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively, in order to micronize the device while preventing a decrease in conductance [Abstract].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the device of Zhu et al. to comprise a vertical channel that has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively, such as taught by Matsuoka, in order to micronize the device while preventing a decrease in conductance.

With respect to claim 11, Zhu et al. discloses a dual-gate field effect transistor according to claim 7. Zhu et al. does not specify that the vertical channel has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively.

However, Matsuoka (Figs. 1(a), 1(b) discloses a vertical channel [15] has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films [17] are in contact with slant faces that are opposed sides of the triangle, respectively [Abstract]. Matsuoka teaches it is beneficial for a vertical channel to have a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively, in order to micronize the device while preventing a decrease in conductance [Abstract].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the device of Zhu et al. to comprise a vertical channel that has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively, such as taught by Matsuoka, in order to micronize the device while preventing a decrease in conductance.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. in view of Mathew et al. as applied to claim 12 above, and further in view of Matsuoka.

With respect to claim 15, Zhu et al. in view of Mathew et al. discloses a dual-gate field effect transistor according to claim 12. Zhu et al. in view of Mathew et al. does not specify that the vertical channel has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively.

However, Matsuoka (Figs. 1(a), 1(b) discloses a vertical channel [15] has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films [17] are in contact with slant faces that are opposed sides of the triangle, respectively [Abstract]. Matsuoka teaches it is beneficial for a vertical channel to have a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively, in order to micronize the device while preventing a decrease in conductance [Abstract].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the device of Zhu et al. in view of Mathew et al. to comprise a vertical channel that has a triangle shape in cross section in the direction orthogonal to the carrier-running direction and wherein the pair of gate insulation films are in contact with slant faces that are opposed sides of the triangle, respectively, such as taught by Matsuoka, in order to micronize the device while preventing a decrease in conductance.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leslie Pilar Cruz/
Examiner, Art Unit 2826

/Evan Pert/
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